REMARKS

In the Office Action, the Examiner noted that claims 1-23 are pending in the application of which claims 9-16 are withdrawn from consideration. The Examiner rejected claims 1-7 and 17-23. By this response, claims 1 and 17 are amended. In view of the above amendments and the following discussion, Applicants submit that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Thus, Applicants believe that all of these claims are now in condition for allowance.

I. Restriction

The Examiner set forth a restriction requirement between claims 1-8 and 17-23 (Group I) and claims 9-16 (Group II). The Examiner stated that the inventions in Groups I and II are related as subcombinations disclosed as usable together in a single combination. (Office Action, p. 2). Applicants affirm the election of claims 1-8 and 17-23 comprising Group I. Claims 9-16 comprising Group II have been withdrawn.

II. Objections

The Examiner objected to the specification, stating that the title should not be included in the abstract. (Office Action, p. 4). Applicants have amended the specification to remove the title from the Abstract section. Accordingly, Applicants respectfully request that the objection to the specification be withdrawn.

III. Rejection of Claims Under 35 U.S.C. §102

The Examiner rejected claims 1-5 and 17-20 as being anticipated by Horn (U.S. Patent Application Publication 2003/0033374, published February 13, 2003). More specifically, the Examiner stated that Horn discloses receiving specification data including attributes of a memory system and generating a logical description of the memory system in response to the specification data. (Office Action, p. 5). The Examiner stated that the logical description of Horn defines a memory component and a memory interconnection component. (Office Action, p. 5). The Examiner further stated that Horn teaches generating a physical description of the memory system in

response to the logical description, where the physical description includes memory circuitry defined by the memory component and having an interconnection topology defined by the memory interconnection component. (Office Action, p. 5). The Examiner concluded that Horn anticipates Applicants' invention recited in claims 1 and 17. The rejection is respectfully traversed.

Horn discloses a communications core on a single device that includes various components, such as a codec, message processor, instruction and data memory, and a subsystem interconnect. (Horn, paragraph [0040]). Horn further discloses a process for programming the communications core in a programmable logic device. In particular, Horn teaches coding the core using an HDL, synthesizing the HDL to produce a gate-level description (also referred to as a logical description), and physically implementing the gate-level description for a programmable logic device. (Horn, paragraphs [0054] and [0055]; FIG. 10, step 424 "translate design into gates").

Horn does not teach each and every element of Applicants' invention recited in amended claim 1. Namely, Horn does not teach or suggest configuring a memory component and a memory interconnection component of a memory model in response to the specification data to generate a logic view of the memory system. In Horn, the communications core, which includes the instruction and data memory, is coded using an HDL and synthesized to produce logic gates. Thus, in Horn, the memory system (the instruction and data memory) is represented in HDL and then translated into logic gates.

In Applicants' invention, during the configuring step, the specified memory system is not translated into logic gates. Rather, the specification data is used to configure a memory component and a memory interconnection component of a memory model. That is, components of a memory model are tailored to the specified memory system and a logical view of the memory system is generated. The HDL code specifying the instruction and data memory in Horn is not used to configure components of a memory model, as recited in Applicants' claim 1. That is, translation of HDL code representing memory into logic gates does not teach or suggest using memory specification data to configure components of a memory model.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim."

Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984). Since Horn does not teach configuring a memory component and a memory interconnection component of a memory model in response to the specification data to generate a logic view of the memory system, Horn does not teach each and every element of Applicants' claim 1 as arranged therein. Accordingly, Horn does not anticipate Applicants' invention recited in claim 1.

Independent claim 17 recites features similar to those recited in claim 1 emphasized above. For the same reasons discussed above, Applicants contend that Horn does not anticipate claim 17. Claims 2-5 and 18-20 depend, either directly or indirectly, from claims 1 and 17 and recite additional features therefor. Since Horn does not anticipate Applicants' invention as recited in claims 1 and 17, dependent claims 2-5 and 18-2 are also not anticipated and are allowable.

In view of the foregoing, Applicants contend that claims 1-5 and 17-20, are patentable over Horn and, as such, fully satisfy the requirements of 35 U.S.C. §102. Accordingly, Applicants respectfully request that the rejection of such claims be withdrawn.

IV. Rejection Of Claims Under 35 U.S.C. §103

A. Claims 6-7 and 21-22

The Examiner rejected claims 6-7 and 21-22 as being unpatentable over Horn in view of Katayama (United States patent 5,867,180, issued February 2, 1999). The rejection is respectfully traversed.

Katayama generally discloses a unified memory architecture that attaches a specially designed memory chip to an existing attachment point of a computer system. (Katayama, Abstract; col. 2, lines 7-12). The specially designed memory chip integrates bus interface logic and on-chip data intensive computation functions with DRAM memory macros. (Katayama, Abstract).

Claims 6-7 and 21-22 depend from claims 1 and 17 and recite additional features therefor. As discussed above, Horn does not teach or suggest configuring a memory component and a memory interconnection component of a memory model in response to the specification data to generate a logic view of the memory system. Katayama is devoid of any teaching or suggestion of a process for designing a

memory system. Notably, Katayama does not disclose configuring components of a memory model in response to memory specification data to generate a logical view of a memory system. Since neither Horn nor Katayama teach or suggest configuring components of a memory model as recited in Applicants' claims 1 and 17, no conceivable combination of Horn and Katayama renders obvious claims 1 and 17. Therefore, Applicants contend that claims 6-7 and 21-22, which depend from claims 1 and 17, are patentable over the cited references and, as such, fully satisfy the requirements of 35 U.S.C. §103.

B. Claims 8 and 23

The Examiner rejected claims 8 and 23 as being unpatentable over Horn in view of Katayama and in further view of Utas (U.S. patent 6,647,431, issued November 11, 2003). The rejection is respectfully traversed.

Claims 8 and 23 depend from claims 1 and 17 and recite additional features therefor. Utas generally discloses a method and apparatus for handling messages. Utas is devoid of any teaching or suggestion of a process for designing a memory system. Notably, Utas does not disclose configuring components of a memory model in response to memory specification data to generate a logical view of a memory system. Since none of Horn, Katayama, or Utas teach or suggest configuring components of a memory model as recited in Applicants' claims 1 and 17, no conceivable combination of Horn, Katayama, and Utas renders obvious claims 1 and 17. Therefore, Applicants contend that claims 8 and 23, which depend from claims 1 and 17, are patentable over the cited references and, as such, fully satisfy the requirements of 35 U.S.C. §103.

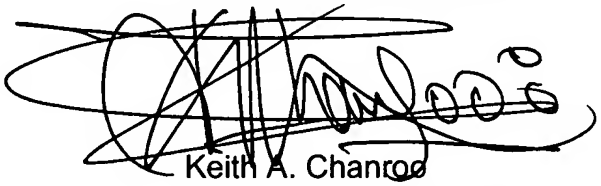
CONCLUSION

Thus, Applicants submit that none of the claims presently in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Consequently, Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Keith A. Chanroo (408) 879-7710 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on August 1, 2006.

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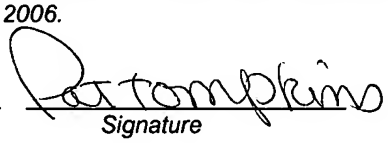

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